DERWENT-ACC-NO: 2001-326282
DERWENT-WEEK: 200207

TITLE: Electrically erasable and programmable read only memory for high-speed
processing, has conductive layer that electrically connects first and second
gate electrodes on main surface of semiconductor substrate

INVENTOR: YOSHIKAWA, K

PATENT-ASSIGNEE: TOSHIBA KK[TOKE]

PRIORITY-DATA: 1999JP-0262717 (September 16, 1999) , 1999JP-0060751 (March 8,
1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6335554 B1	January 1, 2002	N/A	000	H01L 029/788
KR 2000076792 A	December 26, 2000	N/A	000	H01L 027/115
JP 2001156188 A	June 8, 2001	N/A	050	H01L 021/8247

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 6335554B1	N/A	2000US-0521101	March 7, 2000
KR2000076792A	N/A	2000KR-0011598	March 8, 2000
JP2001156188A	N/A	2000JP-0057642	March 2, 2000

INT-CL (IPC): H01L021/8242; H01L021/8247 ; H01L027/10 ; H01L027/108 ;
H01L027/115 ; H01L029/788 ; H01L029/792

ABSTRACTED-PUB-NO: JP2001156188A

BASIC-ABSTRACT: NOVELTY - The EEPROM has a first gate electrode (3) formed on
the main surface of a semiconductor substrate (1) through a gate insulating
film (2). A second gate electrode (8) is arranged on the side of the first
gate electrode through a charge-storing layer (4) placed on the side of the
first gate electrode. A conductive layer (12) electrically connects the gate
electrodes.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the EEPROM
manufacture.

USE - For high-speed processing.

ADVANTAGE - Has simple cell structure for storing several information in bits.
Can be simply manufactured. Ensures high-speed data reading, write-in and
erasing process.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view showing the memory
cell structure of the EEPROM.

Semiconductor substrate 1

Gate insulating film 2

First gate electrode 3

Charge-storing layer 4

Second gate electrode 8

Conductive layer 12

ABSTRACTED-PUB-NO: KR2000076792A
EQUIVALENT-ABSTRACTS: NOVELTY - The EEPROM has a first gate electrode (3)
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US 6335554B

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CHOSEN-DRAWING: Dwg.1/126 Dwg.1/126

TITLE-TERMS:
ELECTRIC ERASE PROGRAM READ MEMORY HIGH SPEED PROCESS
CONDUCTING LAYER ELECTRIC
CONNECT FIRST SECOND GATE ELECTRODE MAIN SURFACE
SEMICONDUCTOR SUBSTRATE

DERWENT-CLASS: U11 U12 U13 U14

EPI-CODES: U11-C18B5; U12-D01A1; U12-D02A2; U12-Q;
U13-C04B1A; U13-C04B2;
U14-A03B7;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2001-327163